REMARKS

By the above amendment, the specification has been amended to correct informalities therein, independent claims 1 and 6 have been amended to correct informalities and in order to recite further features of the present invention as will be discussed below, and dependent claims 2 and 4 have been amended to correct informalities and to clarify features thereof.

Applicants note that although the Examiner refers to a communication filed on 11 December 2001, the communication was filed on December 17, 2001, and included a Preliminary Amendment, Substitute Specification and Proposed Amendment to the Drawings. It is assumed that the Substitute Specification and Preliminary Amendment have been entered, and in light of the new procedures, submitted herewith are corrected drawings corresponding to the proposed amendments submitted on December 17, 2001.

Turning to the amendments of independent claims 1 and 6, applicants note that such claims have been amended to more clearly set forth features of the present invention in relation to the gate line GL as illustrated in Fig. 1 of the drawings as well as the structural arrangement of the semiconductor layer ASI. Submitted herewith is an attached Sketch corresponding substantially to Fig. 1 of the drawings of this application, which has been annotated in accordance with the features now set forth in claims 1 and 6. More particularly, in accordance with the present invention, as illustrated, each of the gate lines has a dimension in a direction of the extension direction of the drain lines (video signal lines) which is substantially constant between adjacent drain lines (video signal lines). Additionally, the semiconductor layer as shown in the attached Sketch has a first portion having the dimension Wα, as shown in the attached Sketch and a second portion having a dimension Wβ, wherein the dimension (Wα) of the first portion in the extension direction of the drain lines (video signal lines) is narrower than a dimension (Wβ) of the second portion in

the extension direction of the drain lines (video signal lines). With this construction as described in the specification of this application, it becomes possible to prevent a photoconducting current produced at the intersection of the gate line and the drain line from affecting the thin-film transistor, as described in the specification of this application. As noted above, each of independent claims 1 and 6 have been amended to recite the aforementioned features and applicants submit that such features are not disclosed in the cited art.

The rejection of claims 1-5 under 35 U.S.C. 102(e) as being anticipated by Ohkawara et al (6,249,325) and the rejection of claims 6-8 under 35 U.S.C. 102(e) as being anticipated by Ohkawara et al (6,504,585), such rejections are traversed insofar as they are applicable to the present claims, and reconsideration and withdrawal of the rejections are respectfully requested.

As to the requirements to support a rejection under 35 U.S.C. 102, reference is made to the decision of In re Robertson, 49 USPQ 2d 1949 (Fed. Cir. 1999), wherein the court pointed out that anticipation under 35 U.S.C. §102 requires that each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. As noted by the court, if the prior art reference does not expressly set forth a particular element of the claim, that reference still may anticipate if the element is "inherent" in its disclosure. To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Moreover, the court pointed out that inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.

The Examiner in applying Ohkawara et al (6,249,325) to claims 1-5 and Ohkawara et al (6,504,585) to claims 6-8 refers to various features of the individual

references, but does not relate the disclosure of such references to the claimed features herein. Accordingly, applicants have experienced difficulty in determining the applicability of the cited art to the claimed invention and, by the present amendment, have recited features, as discussed above, which are clearly not disclosed or taught in such cited art.

Turning to Ohkawara et al (6,249,325) which is applied to claims 1-5, assuming arguendo that Figs. 7(a)-7(d) of the patent may be considered to disclose similar features in relation to the structure claimed in this application, applicants note that while Figs. 7(a) and 7(b) may be considered to disclose a gate line GL having a dimension which is substantially constant between adjacent drain lines, it is readily apparent that Figs. 7(c) and 7(d) show major variations in the aforementioned dimension of the gate line GL, such that it is apparent that this patent and these figures do not disclose the dimension of the gate line being substantially constant between adjacent drain lines, as now recited in independent claim 1 of this application. Furthermore, none of Figs. 7(a)-7(d) of Ohkawara et al (6,249,325) disclose that the semiconductor layer has first and second portions, wherein the first portion has a dimension in the extension direction of the drain line which is narrower than a dimension of the second portion in the extension direction of the drain line. Thus, irrespective of the position by the Examiner, applicants submit that claim 1, as amended, and the dependent claims patentably distinguish over Ohkawara et al (6,249,325) in the sense of 35 U.S.C. 102 and should be considered allowable thereover.

With respect to any contention by the Examiner that Ohkawara et al (6,249,325) is applicable to claims 1-5 in the sense of 35 U.S.C. 103, the Examiner is referred to 35 U.S.C. 103(c) which provides that subject matter developed by another person, which qualifies as prior art only under one or more of subsection (e), (f), and (g) of §102 of this title, shall not preclude patentability under this section

where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. Applicants note that Ohkawara et al (6,249,325) and the present invention are assigned to Hitachi, Ltd., and applicants submit that 35 U.S.C. 103(c) is applicable such that Ohkawara et al (6,249,325) is not available for rejecting claims under 35 U.S.C. 103. Thus, applicants submit that claims 1-5, as amended, patentably distinguish over this cited art and should be considered allowable thereover.

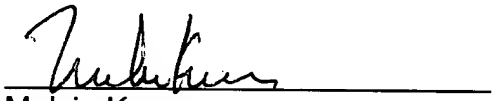
With respect to claims 6-8 and Ohkawara et al (6,504,585) which is utilized under 35 U.S.C. 102(e), applicants note that claim 6 has been amended to in a similar manner to that of claim 1, while utilizing the language of video signal line rather than drain line, noting that such represents the same as is apparent from the description in this application. Irrespective of the position set forth by the Examiner, applicants submit that Ohkawara et al (6,504,585) does not disclose that each of the gate lines has a substantially constant dimension in a direction of extension of the video signal lines between adjacent video signal lines, nor that the semiconductor layer has first and second portions with the dimension of the first portion in a direction of extension of the video signal line being narrower than the dimension of the second portion in the direction of the extension direction of the video signal line. Thus, applicants submit that claim 6, as amended, and the dependent claims patentably distinguish over Ohkawara et al (6,504,585) in the sense of 35 U.S.C. 102, and should be considered allowable thereover.

Applicants further note that with regard to applicability of Ohkawara et al (6,504,585) under 35 U.S.C. 103, applicants submit that 35 U.S.C. 103(c) is applicable thereto in that Ohkawara et al (6,504,585) and the present application are commonly assigned to Hitachi, Ltd., such that this patent is also not utilizable under 35 U.S.C. 103.

In view of the above amendments and remarks, applicants submit that all claims present in this application patentably distinguish over the cited art and should now be in condition for allowance. Accordingly, issuance of an action of a favorable nature is courteously solicited.

To the extent necessary, applicant's petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (501.40175X00) and please credit any excess fees to such deposit account.

Respectfully submitted,



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